

IN THE CLAIMS

1 (Currently Amended). A method comprising:
forming a trench in each of two semiconductor substrates;
providing a catalyst in a ~~the~~ trench; and
combining said substrates in face-to-face abutment with said trenches in alignment with one another.

2 (Original). The method of claim 1 including forming a channel that communicates from opposed ends of each trench to the edge of each substrate to allow fluid to circulate through the substrates via the channels and the trenches.

3 (Original). The method of claim 1 including combining said substrates using copper-to-copper bonding.

4 (Original). The method of claim 3 including masking said catalyst to avoid coating the catalyst with the copper.

5 (Original). The method of claim 4 including lifting off a resist to remove the copper from the catalyst.

6 (Original). The method of claim 1 including depositing the catalyst in the trench.

7 (Original). The method of claim 6 including depositing platinum or lead in said trench.

Claims 8-13 (Canceled).

14 (Currently Amended). A method comprising:
forming a trench in an integrated circuit substrate;
lining the trench with a catalyst material to remove gases from a circulating fluid;

forming channels that align with said trench to allow fluid circulation across said substrate and through said trench; and
protecting said catalyst when forming said channels.

Claim 15 (Canceled).

16 (Original). The method of claim 14 including depositing platinum as said catalyst in said trench.

17 (Currently Amended). The method of claim 14 including depositing lead in said trench as of said catalyst.

18 (New). A method comprising:

combining two semiconductor substrates using copper-to-copper bonding; and
defining a catalyst-filled trench between said substrates.

19 (New). The method of claim 18 including masking said catalyst to avoiding coating the catalyst with copper.

20 (New). The method of claim 19 including lifting off a resist to remove the copper from the catalyst.

21 (New). The method of claim 18 including forming a trench in each of said semiconductor substrates.